Megalithic Microwave Signal Processing for Phased-Array Beamforming and Steering

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***Abstract*— A microwave signal processing (MSP) architecture is presented for active phased array beam forming and steering. A large scale network, comprising 63 power dividers and 32 pairs of vector-synthetic phase/amplitude controllers, has been successfully developed in an 11 mm × 13 mm GaAs monolithic microwave integrated circuit (MMIC). It has a huge integration level of 128 metal–semiconductor field effect transmitters (MESFET's), 448 spiral inductors, 527 metal–insulator–metal (MIM) capacitors, and 357 ion-implanted resistors. The expected 360° phase is successfully obtained at all the output ports. Vector error standard deviations exhibited are within 0.38-dB root-mean square (rms) and 2.8° rms over the bandwidth of 20 MHz at 2.5 GHz. This megalithic chip could mark an epoch in phased array systems.**

***Index Terms*—Active phased arrays, beamforming, cold FET's, microwave attenuators, microwave phase shifters, microwave signal processing, MMIC's, power dividers/combiners, satellite communication onboard systems, varistors, wafer-scale integration.**

I. Introduction

TRANSMITTED power requirements in satellite communication systems have been steadily increasing in recent years, and the numbers of satellite beams is also predicted to increase annually because of frequency reuse and the growing traffic demand. As a means of meeting these requirements, global and regional access satellite communication systems featuring multiple-beam LEO or GEO satellites have recently been proposed. In developing satellite of this type, the use of an active phased array with spatial power combining is considered a viable means of enabling the radiation of high-power multiple beams. In this approach, the beamforming network (BFN) is expected to provide the following functions:

1) precise pointing of each beam to the target area despite possible deviations of the array system components and satellite attitude;
2) forming of nulls exactly onto the neighboring area where frequency reuse could create problems;
3) providing of reconfiguration in case a failure occurs in any radiated beam.

Precise beam and null pointing is especially important in high-gain reflector antenna systems [1]. Digital beamforming (DBF) or digital signal processing (DSP) has been employed in some practical systems [2], [3] to achieve adaptive beam steering. In multi-carrier systems such as satellite transponders, however, DSP dissipates a large amount of dc power as the number of the carriers increases. It also requires dozens of high-speed and high-resolution digital-to-analog converters (DAC's).

Another approach to beam steering is to introduce control circuits [4]–[9] in an analog BFN. This paper presents a direct microwave signal processing (MSP) architecture which employs this approach to achieve active phased array beamforming and steering. The architecture's highly dense constituent circuit topologies and the superior megalithic integration achieved with it are described.

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II. BFN Architecture

The BFN is the key device for achieving an active phased array. Butler's hybrid matrix network [10] is commonly used as BFN architecture, because it can create multiple beams simultaneously with a limited scale microwave circuit. Unfortunately, the hybrid matrix is useful only for fixed beamforming and is unable to steer each beam (see Table I). To steer each beam independently, the BFN must distribute the RF input signal to all the radiators with a specific phase. Each distributed and weighted signal has to be combined with the signals of other beams. Amplitude is also controlled for beam pattern shaping and side lobe suppression. Therefore, the BFN must be equipped with a proportional number of power divider/combiners, variable phase shifters, and attenuators to the number of beams times the radiator elements. The MSP should have the following functions:

input—division—complex weighting—combining—output.

An interconnected three-dimensional (3-D) structure [11] loaded with N GaAs monolithic microwave integrated circuit (MMIC) chips followed by M sets of N-way passive combiner substrate is proposed to form a compact hardware (see Fig. 1). M and N are the number of radiators and beams, respectively. Since the beamforming function for each beam is integrated in a single chip, we label this BFN configuration "single-chip-per-beam." Monolithic integration of this huge scale circuit is achieved through a new MSP architecture as shown in Fig. 1, featuring a 64-way pyramidal power distribution and phase/amplitude control without employing any conventional phase shifters. Full 360° phase is generated on a

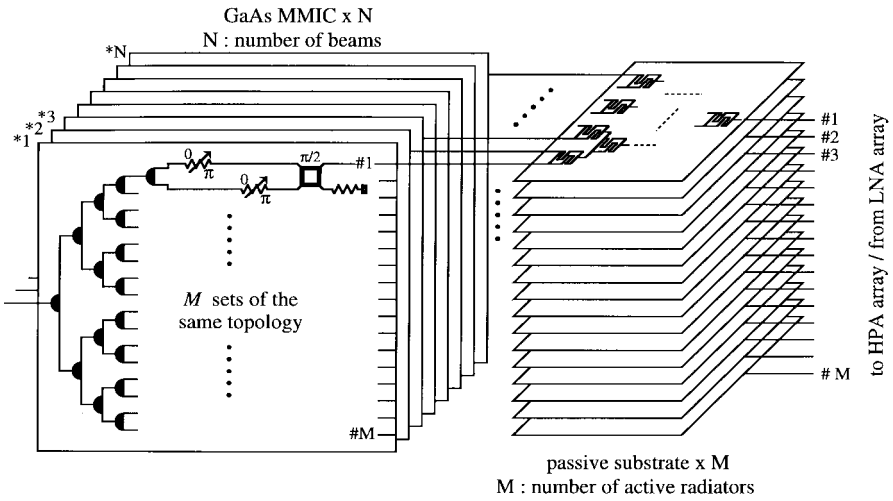


Fig. 1. Proposed $M \times N$ multiple-beamforming and steering network architecture. Main features: 1) very high-level integration, i.e., all the control circuits for each beam are in a single GaAs MMIC chip and 2) unique circuit topologies for pyramidally cascadable power divider and M-parallel vector-synthetic amplitude/phase controllers.

TABLE I

		separate	multi-port transmitter	active phased array transmitter		
Configuration		SW	SW BM BM	SW BM	MSP	DSP DAC DAC DAC
Signal processing		N/A	microwave high-level stage	microwave low-level stage		base-band or IF low-level stage
Power combining		N/A	in-circuit combining	spatial power combining		
Power flexibility		limited by each PA	automatically assigned according to the traffic			
Beam steering		discrete switching among fixed beams			continuous and independent beam steering	
Phase adjust		N/A	hardware cut-and-try trimming		electronically programmable	
Power dissipation or heat generation	DC	N/A	none		very low	fairly high due to high-resolution high-speed multiple DACs
	RF	N/A	high due to multi-stage hybrid matrix	very low		N/A

SW: switch matrix, BM: butler matrix, DAC: digital-to-analog converter, MSP: microwave signal processing, DSP: digital signal processing.

vector-synthetic or vector-modulator principle by orthogonally coupled twin attenuators. The proposed circuit topologies to achieve this architecture are the pyramidally cascadable power divider (PcPD) and the phase-invertible variable attenuator (PiVA).

III. Pyramidally-Cascadable Power Divider (PcPD)

The Wilkinson power divider/combiner is well known and widely used as the key basic three-port constituent passive device for MIC's and MMIC's. The device's unique feature is that it provides two-way signal distribution with completely symmetrical amplitude and phase. It also features excellent isolation between its two output ports as well as simultaneous impedance matching at all three of its ports. In spite of its advantages, the Wilkinson divider is composed of quarter wavelength long distributed-constant transmission lines resulting in large physical space; thus its topology is not practical for monolithic integration, especially at lower frequencies. Various attempts such as folded microstrip [12], quasi-lumped circuit [14], and a 3-D MMIC approach [22], have been reported to reduce the size of passive basic circuits. Even though these techniques brought considerable size reduction in comparison with the conventional quarter wavelength circuit (Fig. 2), much more reduction is required for MSP. As a means of achieving this, we present a novel and simple circuit configuration for the cascaded signal division. The key technical point is how to simplify the circuit configuration without sacrificing electric performance, e.g., impedance matching, insertion loss, and isolation between output ports. The complex iterative impedance method is introduced as a useful technique to meet these opposing requirements.

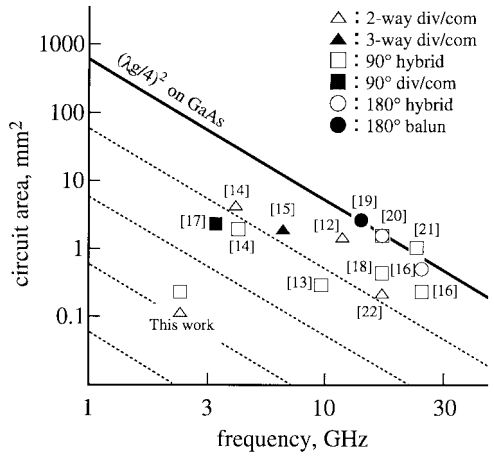


Fig. 2. Passive circuit size reduction for high-integration MMIC's.

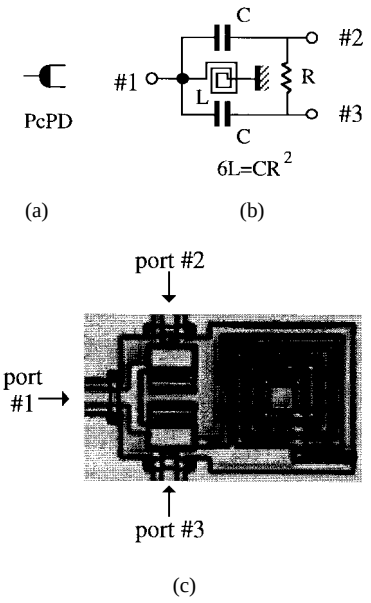


Fig. 3. Pyramidally cascadable Power Divider (PcPD). (a) Symbol. (b) Schematic diagram. (c) Prototype fabricated on GaAs substrate. Size: 0.12 mm^2.

In lumped-element MMIC layouts, spiral inductors often occupy much more area than capacitors or resistors. This is physically inevitable because the substrate material, e.g., GaAs, is not a magnetic medium, while capacitors employ a highly permittive medium in their interelectrode insulators. An effective design solution for high density MSP is to reduce the total number of inductors and the absolute inductance value of each inductor. The circuit topology proposed here, shown in Fig. 3, employs only one inductor, whose inductance is one third of that used in the previously reported configuration [14]. It is a drastically simplified design topology, yet it keeps the basic characteristics of simultaneous three-port impedance matching, symmetrical two-way power division, and isolation between two output ports, if $6L = CR^2$. (See the Appendix for details.)

We developed a prototype circuit designed to function at 2.5 GHz ±10 MHz, i.e., S-band communication satellite frequency. The element constants determined are $R = 100\ \Omega$, $L = 1.5$ nH, and $C = 0.9$ pF. Fig. 3(c) shows a prototype of the circuit fabricated on a GaAs substrate; occupies only 0.12 mm^2 of MMIC space. This circuit is believed to be the smallest power divider ever reported at this frequency (Fig. 2). This design enables us to achieve a 2^n-way pyramidal power distribution in a very compact area.

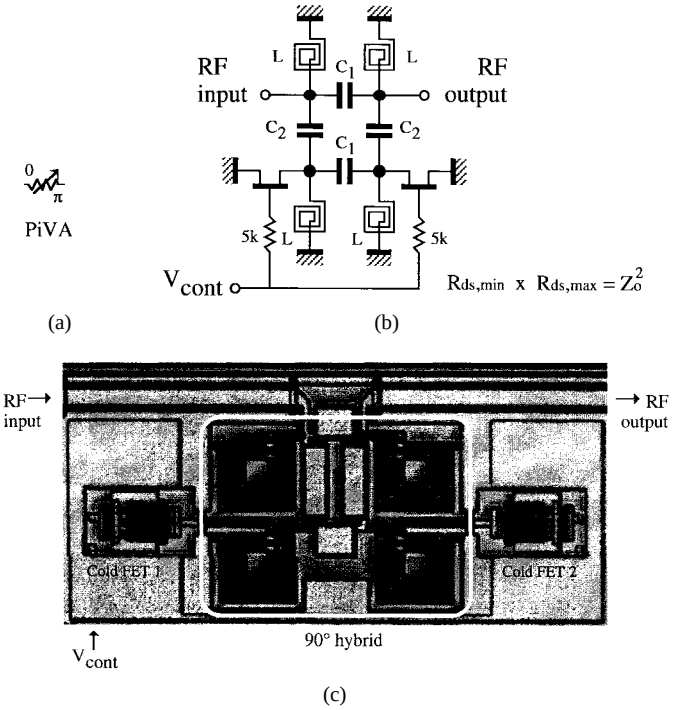


Fig. 4. Phase-invertible Variable Attenuator (PiVA). (a) Symbol, (b) schematic diagram, and (c) prototype fabricated on GaAs substrate. It measures 0.64 mm^2, including the $\pi/2$ hybrid (0.24 mm^2: inside the white line), twin FET's and I/O feed lines. The FET's are called "cold FETs" since they have zero dc drain–source voltage and zero dc gate current.

IV. Phase-Invertible Variable Attenuator (PiVA)

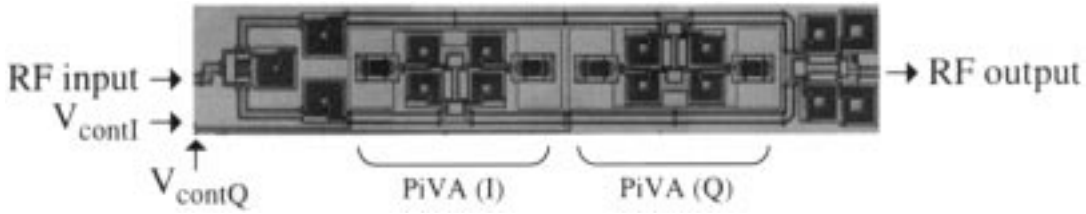
The next approach is to combine a number of functions in a single circuit. The proposed circuit topology, PiVA, performs continuously variable attenuation and π phase inversion. The concept of PiVA, shown in Fig. 4, utilizes a pair of cold FET's interlocked by a single control voltage. To carry out the phase inverter function, the gate width is designed to satisfy the relationship:

$$R_{\mathrm{ds,\,min}} < Z_o < R_{\mathrm{ds,\,max}}$$

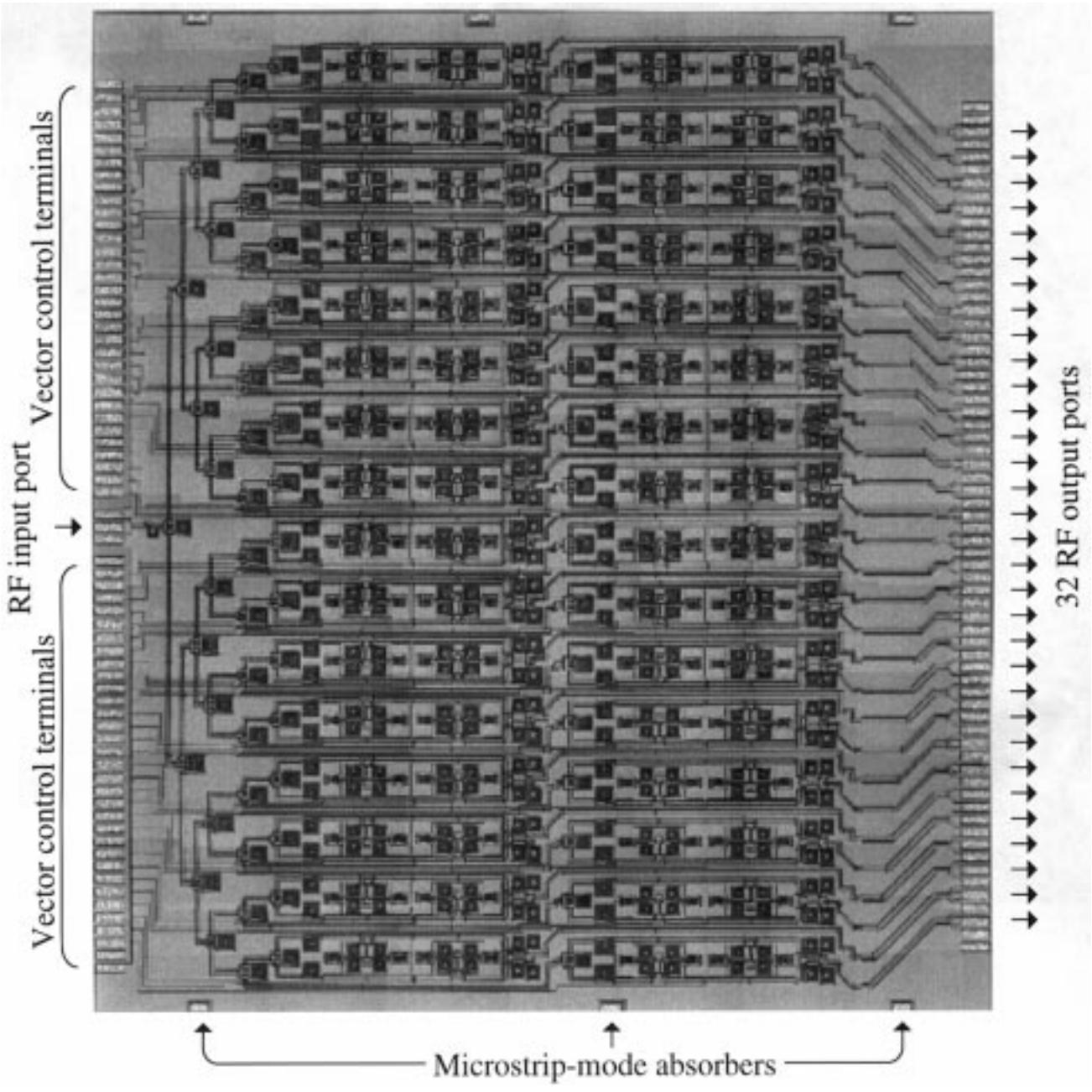
where R_{ds} is the drain–source variable resistance of the cold FET and Z_o is the characteristic impedance of the 90° hybrid achieved using the L and C components. With the help of circuit symmetry [23], the lumped constants are deduced in the same manner as the PcPD, cf. the Appendix, resulting in

$$C_1 = \frac{1}{\omega Z_o}, \quad C_2 = \frac{\sqrt{2}}{\omega Z_o}, \quad L = \frac{1}{1+\sqrt{2}}\,\frac{Z_o}{\omega}.$$

The forward transfer phase $\angle S_{21}$ exhibits ±90° phase shift when $R_{\mathrm{ds}} < Z_o$ or $R_{\mathrm{ds}} > Z_o$, respectively. The key design point is to obtain symmetrical attenuation characteristics



(a)



(b)

Fig. 5. View of the developed prototype GaAs megalithic BFN. (a) A vector synthesizer portion for attaining an orthogonal and complete constellation, i.e., full 360° phase and arbitrary amplitude control and (b) an entire microwave signal processing function for 32-element phased-array beamforming/steering integrated in an 11 mm × 13 mm MMIC chip.

between the two phase states such that

$$R_{\mathrm{ds,\,min}} \times R_{\mathrm{ds,\,max}} = Z_o^2.$$

A PiVA prototype matching that of PcPD was developed and also designed to function at 2.5 GHz ± 10 MHz. To minimize the inductance, characteristic impedance is maintained at the low level of as $Z_o = 33.3\ \Omega$, resulting in $L = 0.85$ nH, $C_1 = 1.9$ pF, and $C_2 = 2.7$ pF. In the fabricated prototype, shown in Fig. 4(c), the PiVA occupies only 0.64 mm^2 of the GaAs substrate. This cell requires only one control signal, hence it is

very space efficient. Based upon the vector-synthetic principle, arbitrary phase and amplitude is generated by orthogonally combining a pair of PiVA cells. The complex transfer function S_{21} of the combined circuit is formulated as

$$S_{21} = \frac{1}{2}\left(\frac{R_{\mathrm{ds},1} - Z_o}{R_{\mathrm{ds},1} + Z_o} + j\,\frac{R_{\mathrm{ds},2} - Z_o}{R_{\mathrm{ds},2} + Z_o}\right)$$

where $R_{\mathrm{ds},1}$ and $R_{\mathrm{ds},2}$ are the drain–source resistances of the cold FET's used in each PiVA cell. These resistances are controlled by a pair of external dc voltage supplies. This vector-synthetic phase generator is more linear than other phase shifters [7] based on varactor diodes, since the nonlinear Schottky-junction capacitances introduce intermodulation distortion.

V. Prototype GaAs MMIC

Utilizing the high-integration circuit topologies proposed in the two previous sections, a prototype "single chip per beam" BFN is fabricated on an 11 mm × 13 mm GaAs substrate as shown in Fig. 5. It consists of:

1) one RF input port;
2) a six-stage pyramidal divider;
3) 32 sets of vector synthesizers;
4) 32 RF output ports;
5) 32 pairs of control dc terminals;
6) peripheral ground terminals.

The 32-way divider provides uniform-phase and uniform-amplitude signals. Amplitude and phase of each signal are controlled in the vector synthesizer stage. The integrated elements total more than one thousand, i.e., 128 metal–semiconductor field effect transmitter (MESFET's), 448 spiral inductors, 527 metal–insulator–metal (MIM) capacitors, and 357 ion-implanted resistors. To accomplish this high integration level, a coplanar structure is employed which eliminates via holes. To suppress unwanted microstrip-mode resonance, Q-damping elements are placed on the edge of the chip.

VI. Test Procedure and Results

The megalithic BFN performance was measured at the S-band satellite communication frequencies using a wafer probe station. The DUT has 1 input port and 32 output ports. A custom-built multiple-port probe card was employed to measure the [S] parameters at the port under test as well as to terminate the other 31 ports. Thus, a two-port network analyzer is used sequentially port by port. Two dc voltage supplies are necessary to control the output vector, in-phase and quadrature, for each port.

First, port 1 was tested while the others are terminated to 50-Ω loads. The control voltages were imposed only for port 1. The voltages were adjusted so as to obtain endless phase shift in a constant amplitude. The expected 360° phase was successfully attained, as depicted in the polar plot of Fig. 6(a) in 15° steps. In each of the 24 states, phase variation was measured and is depicted in Fig. 6(b) as a function of frequency. The phase differences between two adjacent states are held almost constant in this frequency range.

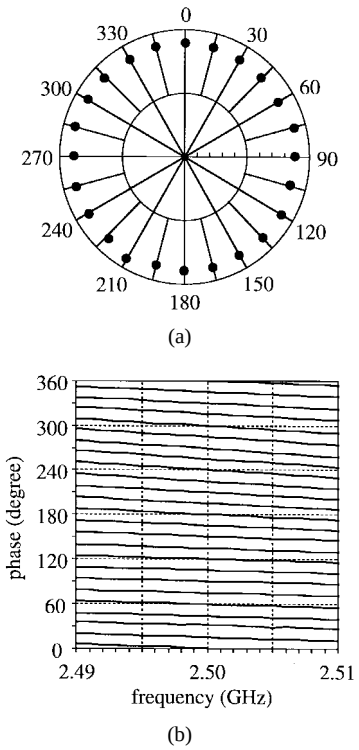


Fig. 6. The measured phase control performance of the megalithic BFN. (a) Representations of a full 360° vector synthesis in 15° steps measured at the center frequency and (b) measured phase variation as a function of frequency over the 24 phase states.

Next, the orthogonal control voltages were swept over their full span to observe the entire constellation. The synthesized vector for this two-dimensional (2-D) trace is plotted as shown in Fig. 7. It demonstrates an orthogonal and complete constellation. This vector synthesis test was completed at ports 1–32. No defects were found at any port.

Then, full-32-port amplitude/phase adjusting was attempted. For automatic measurement and adjusting, a setup composed of a vector network analyzer, 32 pairs of GP–IB controlled dc voltage supplies, and a control computer were added to the wafer probe station. The 32 pairs of amplitude/phase targets are obtained from the system requirements. The supply voltages are sequentially controlled by the computer to minimize the differences:

$$\Delta a_i = a_i - \alpha_i \text{ and } \Delta\varphi_i = \varphi_i - \Phi_i; \qquad i = 1, 2, 3, \cdots, M$$

where a_i and φ_i are measured values, α_i and Φ_i are the given target for the ith port, and M is the number of ports ($M = 32$). Some errors are caused by the mutual electromagnetic coupling between adjacent output ports since they lie densely side by side as shown in Fig. 5. These errors are serious when accuracy is required in the phased array system. The computer algorithm to overcome this problem is shown in Fig. 8. In this flow chart, the inner feedback loops reduce the errors in each port. The outer feedback loop reduces the errors due to the mutual coupling. A 2-D modified Newton method is employed in fine voltage adjusting for each port. Using this iterative method enabled the correlated errors to be removed. All that remains are the residual random error, which was a very low 0.1-dB rms and 0.7° rms at the center frequency.

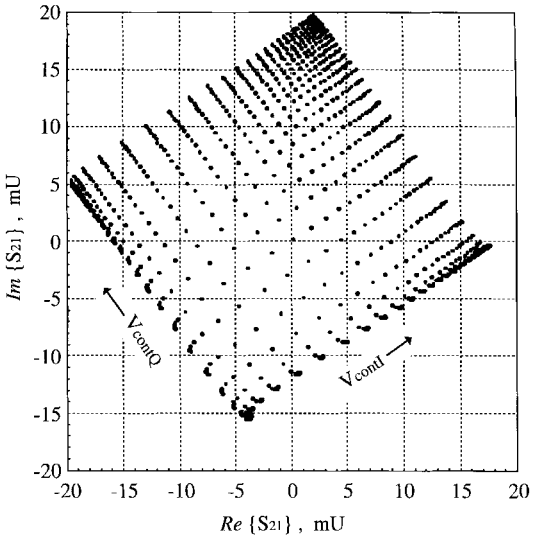


Fig. 7. Constellation of the synthesized vector observed at port 1: The parameter S_{21} is measured and plotted in the real-imaginary chart. The unit mU is used for $\times 10^{-3}$. The in-phase and quadrature control dc voltages ($V_{\mathrm{cont}\,I}$ and $V_{\mathrm{cont}\,Q}$) are swept over the span of 0 to -1.5 V with the step of 50 mV. The constellation is skewed from the axes because of a fixed phase delay between the input and output ports. The nonuniform density of points comes from the dc control characteristics of the attenuators. This square shape is good in its orthogonality and completeness.

Finally, all the supply voltages were set at the above converged voltage levels, and the vector variation versus frequency was measured for all the ports. At each frequency, the 32 vector errors, i.e., Δa_i and $\Delta\varphi_i$; $i = 1$ to 32, were statistically evaluated by using the standard deviations defined as

$$\sigma_{\Delta a} = \frac{1}{M}\sqrt{M\sum_{i=1}^{M}\Delta a_i^2 - \left(\sum_{i=1}^{M}\Delta a_i\right)^2}$$

$$\sigma_{\Delta\varphi} = \frac{1}{M}\sqrt{M\sum_{i=1}^{M}\Delta\varphi_i^2 - \left(\sum_{i=1}^{M}\Delta\varphi_i\right)^2}.$$

The resultant vector deviations are within 0.38 dB rms and 2.8° rms over the bandwidth of 20 MHz at 2.5 GHz as shown in Fig. 9. The dc current observed at each control terminal is less than 50 μA throughout this test because of the very high dc gate impedance of cold FET's.

This performance is suitable for onboard active phased array applications. The designed BFN is fully reciprocal so that it can be applied not only to transmitters but also to receivers. Since this design is both space efficient and nonheat-generating, it could be applied to multibeam BFN's by piling up the BFN chips with high-isolation packages [11] for each beam control layer as shown in Fig. 1.

VII. Conclusion

Several novel lumped-constant circuit topologies have been presented for high density integration. An innovative huge scale circuit, being fully functional as a beamforming and steering network, has been designed and fabricated in a single GaAs MMIC chip. In spite of this huge scale of integration, no defects were found on the chip. Full 360° phase was observed at the target frequency. The expected vector synthesis was successfully completed at all the output ports. Amplitude and phase are controlled by the computer program to converge onto the target accurately with a double-closed-loop iterative algorithm. Residual error was a low 0.38 dB rms and 2.8° rms in the 20 MHz at S-band range. The chip is ready to go onboard for practical communication satellites. This megalithic development can be a major step toward achieving "pseudo-" LSI signal processing directly at microwave frequencies. Unlike DSP or DBF, which need many high-speed DAC's, this MSP architecture can carry out adaptive beamforming functions with very low dc-power consumption. It is free from both Nyquist sampling speed and quantization error. It is potentially a significant step in the

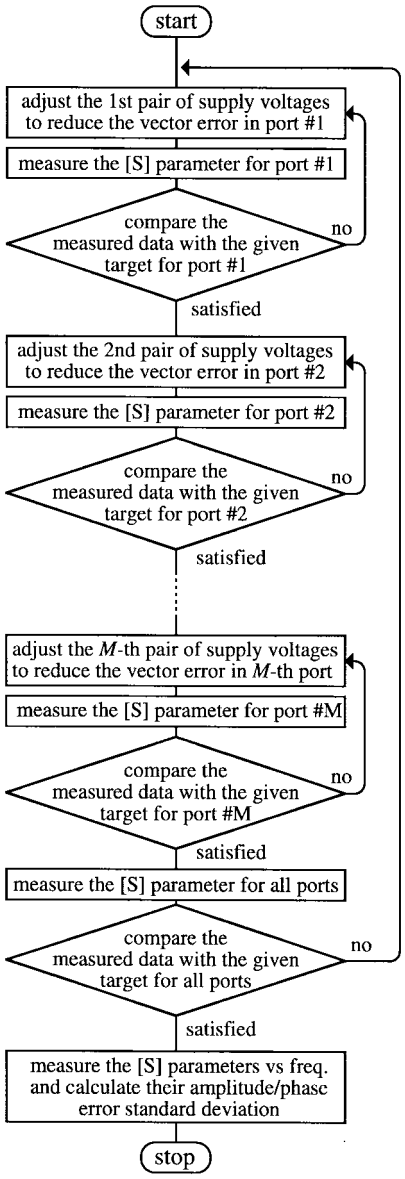


Fig. 8. Double-loop feedback algorithm for full-M-port amplitude/phase adjusting: The inner feedback loops reduce the errors in each port. The outer feedback loop reduces the errors due to mutual coupling between adjacent ports.

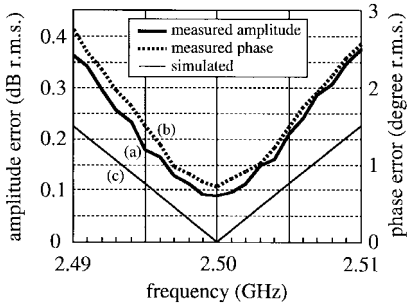


Fig. 9. Synthesized vector accuracy of the megalithic BFN. The standard deviations of amplitude and phase errors measured for the 32 output ports are designated by (a) and (b), respectively. The circuit simulator estimates the amplitude and phase deviations resulting in the degenerated line (c). The ordinates for amplitude and phase errors have the scales that indicate equivalent effects [24] on the radiation pattern in phased array antennas.

ongoing development of multiple-carrier transmitting phased arrays in low intermodulation distortion communication channels, and of GEO/LEO satellite onboard active phased array transponders.

APPENDIX

To cascade circuits directly one after another without interstage matching networks, an "iterative impedance" technique is introduced. Iterative impedance is defined as "the input impedance of the circuit when all the output ports are terminated to the loads which have the same impedance as the input port of the circuit itself." The iterative impedance, Z_{itera}, is formulated as

$$Z_{\text{itera}} = Z_{\text{input}}\big|_{Z_{\text{load}}=Z_{\text{input}}}$$

and

$$Z^*_{\text{itera}} = Z_{\text{output}}\big|_{Z_{\text{source}}=Z_{\text{output}}}$$

where the asterisk (*) denotes the complex conjugate. Once the circuit finds a Z_{itera} satisfying the first formula, the second formula is accordingly satisfied at least for reciprocal networks. In this definition, it is clear that the circuit is cascadable if and only if there exists an iterative impedance for the circuit. Herein "cascadable" means being able to connect each stage after another stage. Fortunately, the circuit shown in Fig. 3 has an iterative impedance, which is analytically deduced and found to be a complex number as shown below.

Let all the two output ports be terminated to some unknown load impedance Z_{load} as shown in Fig. 10. Looking into port 1, the circuit is equivalent to the schematic shown in Fig. 10(a), thanks to circuit symmetry [23]. The input impedance Z_{input} is calculated as:

$$Z_{\text{input}} = \frac{1}{\dfrac{1}{\dfrac{1}{2}Z_{\text{load}} + \dfrac{1}{2j\omega C}} + \dfrac{1}{j\omega L}}.$$

Imposing the cascadable condition into the above, an equation for Z_{itera} is obtained as

$$j\omega C Z^2_{\text{itera}} + (1 - \omega^2 LC) Z_{\text{itera}} - j\omega L = 0. \tag{A1}$$

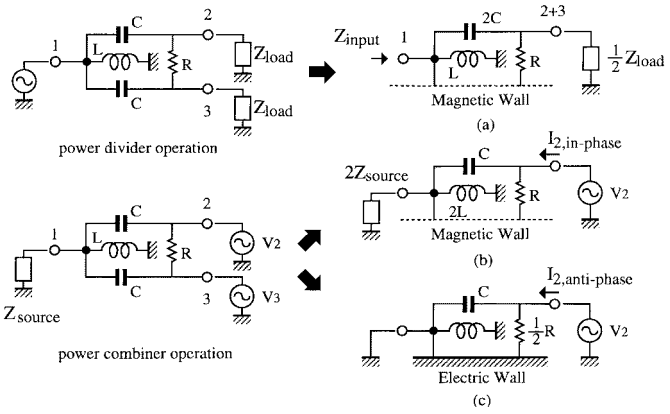


Fig. 10. Analysis on complex iterative impedance for the PcPD. For power divider operation, input impedance is calculated by the even-mode equivalent circuit shown in (a). Power combiner operation is regarded as superposition of even- and odd-mode operations as shown in (b) and (c). The in- and antiphase components of current I_2 are calculated by exciting $V_2 = V_3 = 1$, and $V_2 = -V_3 = 1$, respectively. Internal impedance of each voltage source is omitted for simplicity.

This equation has two complex solutions for Z_{itera}. The one that has a positive real part should be preferred for passive impedance matching.

The next step we proceed is to isolate the two output ports. Terminating port 1 with unknown Z_{source}, this circuit is regarded as the two-port network shown in Fig. 10. The current at port 2 is expressed using admittance parameters as $I_2 = Y_{22}V_2 + Y_{32}V_3$. With the help of topological symmetry [23] again, the circuit is equivalent to Fig. 10(b) or (c) for in- or antiphase unity voltage excitations, respectively. Therefore, the current I_2 is calculated for each excitation as

$$I_{2,\,\text{in-phase}} = \frac{1}{\dfrac{1}{\dfrac{1}{2Z_{\text{source}}} + \dfrac{1}{2j\omega L}} + \dfrac{1}{j\omega C}}$$

and

$$I_{2,\,\text{antiphase}} = j\omega C + \frac{2}{R}. \tag{A2}$$

To isolate ports 2 and 3 from each other, the cross term Y_{32} should vanish or

$$I_{2,\,\text{in-phase}} = Y_{22} = I_{2,\,\text{antiphase}}. \tag{A3}$$

Another condition we should apply is the output impedance matching

$$Z_{\text{source}} = 1/Y^*_{22} \tag{A4}$$

where the asterisk (*) denotes the complex conjugate. Substituting (A2) and (A4) into (A3), the unknown source is eliminated and the resultant formula deduces a simple relationship as

$$6L = CR^2 \text{ and } 3\omega^2 LC = 1. \tag{A5}$$

Simultaneous solutions of (A5) provide element values for the center frequency. In case that the center frequency is given first, L and C are explicitly calculated by

$$L = \frac{R}{3\sqrt{2}\omega} \text{ and } C = \frac{\sqrt{2}}{\omega R}.$$

The resistance R is not restricted here but should be optimized so that both L and C fall into practically available values. For example, $R = 100\ \Omega$ is preferred for S-band applications, resulting in $L = 1.5$ nH and $C = 0.9$ pF at 2.5 GHz.

The final step of the formulation deduces the iterative impedance. To solve (A1) for Z_{itera}, (A5) is used and the L and C are then eliminated. From the two possible complex solutions, we prefer the one which has the positive real part. Consequently the iterative impedance is found to be a complex number

$$Z_{\text{itera}} = Z_{\text{load}} = Z_{\text{input}} = \frac{2 + j\sqrt{2}}{6} R.$$

It goes without stating that Z_{source} or Z_{output} is conjugate to the above impedance, since this two-way divider/combiner is obviously a reciprocal circuit. The sign of the imaginary part means that the circuit has inductive input and capacitive output impedances.

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